Apricot Expansion Boards

Contents

1 General Installation Instructions.

1. General Recommendations
2. Apricot PC - Apricot Xi
3. Apricot F1 - Apricot F1e
4. Apricot Portable

1. General Recommendations

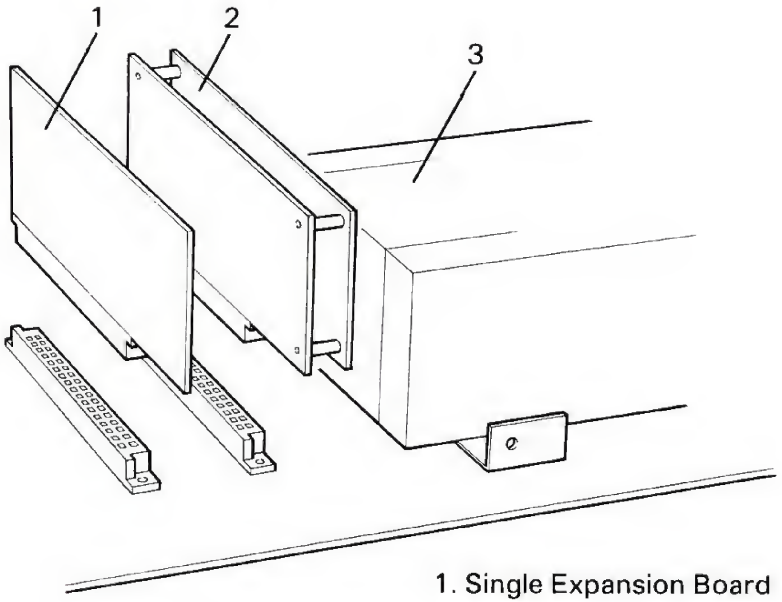
1. It is recommended that installation of any expansion board be carried out by an authorised dealer.

   Warning - Remove Power Cable Before Attempting To Gain Access To The Expansion Slots.
2. Unless specifically noted, assembly is the reverse of disassembly.
3. Do not mix screws (length, diameter).
4. A number in parenthesis, thus (4) indicates the number of screws to be slackened or removed to remove that particular part.
5. The expansion slot is polarised to prevent incorrect insertion.
6. A single or double board may be installed into any Apricot.
7. Check all expansion board pins are straight before fitting into expansion slot.
8. Plug in all cables as per relevant instructions and jumper pins where necessary.

2. Apricot PC - Apricot Xi

Removal of top cover.

1. Remove M4 x 12mm screws (3) on rear panel.
2. Allow rear panel to tilt backwards and remove top cover by lifting at rear slightly and disengaging lip from front bezel.
3. Expansion slots are adjacent to power supply.



1. Single Expansion Board
2. Double Expansion Board
3. Power Supply

When installing a single layer board, i.e., a ram expansion, the board may be plugged into any of the expansion slots.

When installing an option with a daughter board attached, i.e., a colour or modem card, then it must be plugged into the slot adjacent to the power supply as shown above.

Plug in all cables as per relevant instructions and jumper pins where necessary.

The expansion plates on the rear panel may be pushed out if applicable.

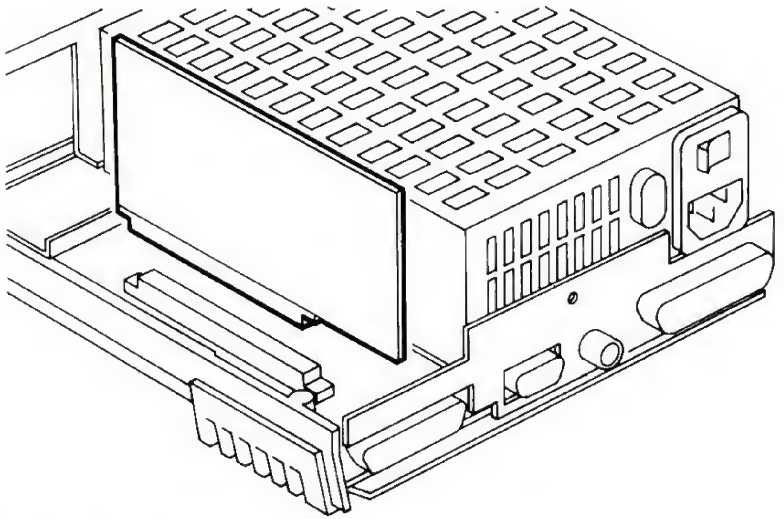
Assemble machine as per previous instructions.

Refer to relevant section in this chapter regarding specific installation instructions.

3. Apricot F1 - Apricot F1e

Removal of top cover

1. Remove M3 x 10mm screws (2) on rear panel.
2. Allow rear panel to tilt backwards and remove top cover by lifting at rear slightly and disengaging lip from front bezel.
3. Expansion slot is adjacent to the power supply.



Plug in all cables as per relevant instructions and jumper pins where necessary.

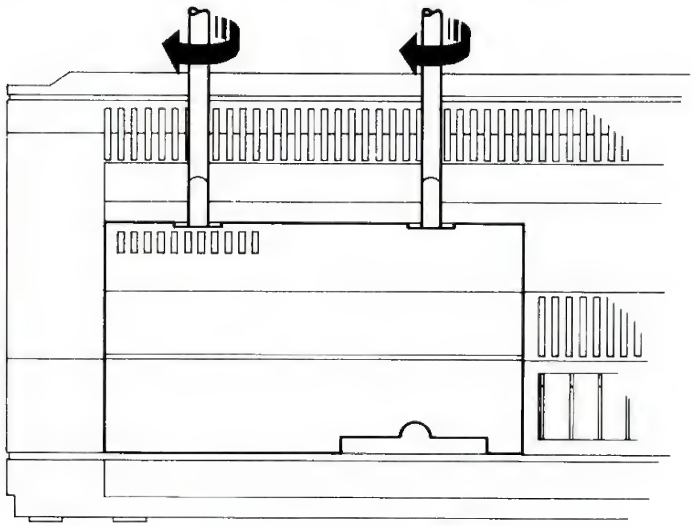
The expansion plate on the rear panel may be pushed out if applicable.

Assemble the machine as per previous instructions.

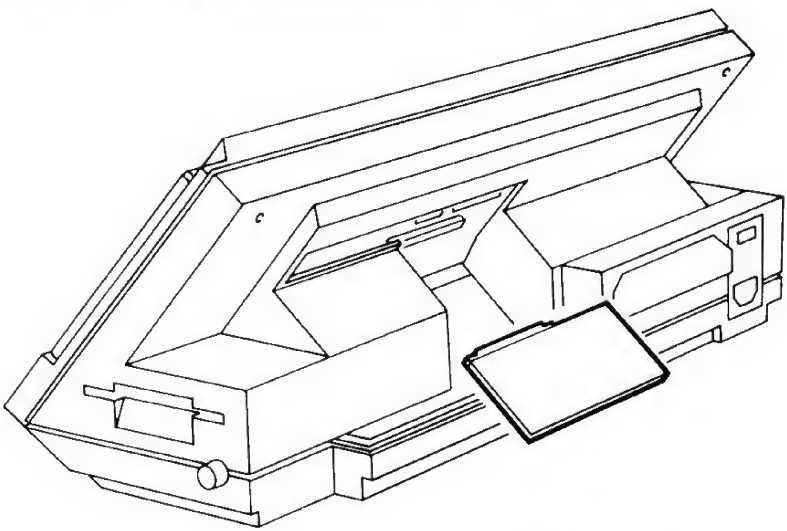
Refer to relevant sections in this chapter regarding specific installation instructions.

4. Apricot Portable

Removal of Apricot Portable cable manager



Installation of expansion board into Portable



When installation is complete clip the cable manager in place.

2 Power Requirements

Expansion Board	+5u	Construction
128K RAM	0.5A	Single
256k RAM	0.5A	Single
512K RAM	0.49A	Single
Lan	0.35A	Single
Winchester	0.6A	Single
Modem	0.37A	Double
Colour	1.3A	Double

256K RAM Expansion Board 3

1. Installation
2. Theory of operation.
3. Integrated circiut catalogue.
4. Mnemonics
5. Parts list.

1. Installation

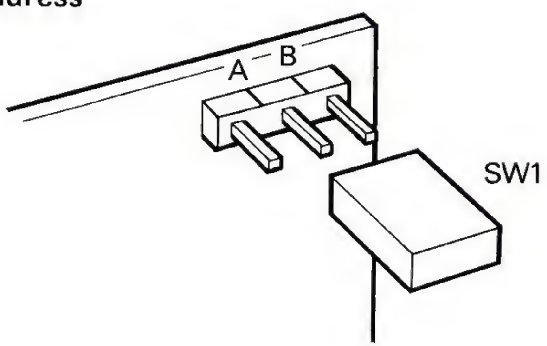
256K RAM expansion boards may be installed into the Apricot range. The Apricot PC/Xi range may have 1 or 2 boards fitted making a total capacity of either 512k or 768k.

NOTE This board can not be fitted to an F1e.

Any expansion slot may be used for individual boards.

A general description of installation procedure is contained at the beginning of this section.

Base Address



A jumper SW1 is provided, as detailed above, to set a base address for the board, of either 40000H or 80000H. Jumper 'B' when one board is installed and 'A' on the second, when two boards are fitted.

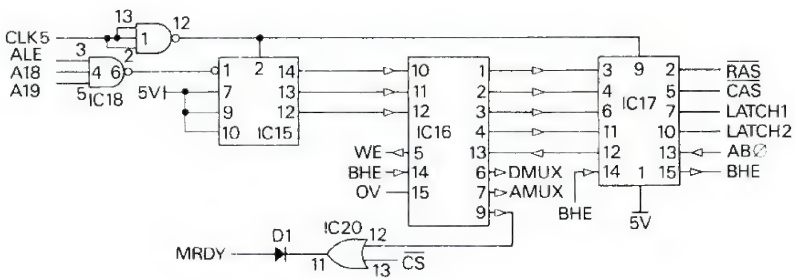
2. Theory of Operation

The design utilizes 8 256K x 1 dynamic ram chips (ICI-IC8) with on chip refresh. This allows most of the logic associated with the DRAM refresh function to be eliminated from the design.

The 16 bits of data is multiplexed onto an internal 8 bit wide data bus via IC11 and IC12 under the control of DMUX. Data from the ram chips is latched in as upper and lower bytes into IC9 and IC10. Latching is accomplished at the correct time by LATCH1 and LATCH2. Similarly, the address bus AB1-AB16 is multiplexed onto an internal 8 bit wide address bus via IC13 and IC14 under the control of AMUX.

IC19 with inputs DMUX and AB17 controls the selection of high or low memory pages. Board selection via SW1 is generated by the IC18 and IC19 combination, resulting in CS.

Timing for the circuit is accomplished using a counter, PROM and latch (IC15, IC16, IC17) in a novel form as shown below.



A valid CPU memory cycle synchronizes a 3 bit counter (IC15) by clearing it to zero during an ALE pulse, clocking of the counter is by CLK5. During each CPU memory cycle, IC15 counts from 0 to 7 and drives a PROM (IC16) - this chip is programmed with all the control signals necessary to access the memory and maintain DRAM refresh, even during repetative memory accesses.

3. Integrated Circuit Catalogue

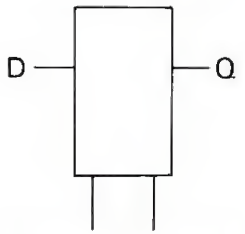
IC	1,2,3,4,5,6,7,8.

HM50256-20 256K x 1 Dynamic Random Access Memory.

Forms 256K x 8 memory

IC	9,10

74LS373 'D' Type Latches



Function Table			
Output Control	Enable G	D	Outputs
L	H	H	H
L	H	L	L
L	L	X	Q
H	X	X	Z

Latches high and low order bytes to main data bus during a memory read, under control of LATCH1, LATCH2, C5 and MRDC.

IC	11,12,13,14.

74LS257 Multiplexers

Function Table				
Inputs		Outputs Y		
Output Control	Select	A	B	LS257A
H	X	X	X	Z
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

IC	11,12.

Multiplexes 16 data bits onto 8 bit DRAM data bus during a memory write, under control of DMUX.

IC	13,14.

Multiplexes 16 address bits onto 8 bit DRAM address bus under control of AMUX.

IC	15.

74LS163 Synchronous 4 Bit Counter

Counts from 0 to 7 under control of ALE, A18, A19 and clocked by CLK5. Generates input signals for PROM (IC16).

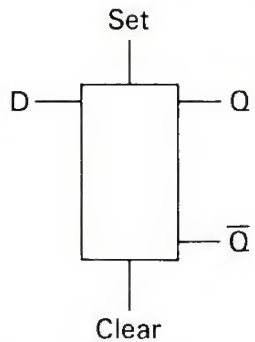
IC	16.

74S288 256 Bit Programmable Read-Only Memory

Programmed with control signal and timing information.

IC	17.

74LS174 'D' Type Flip-Flop

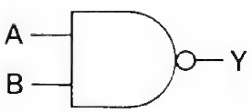


Function Table					
Inputs				Outputs	
Preset	Clear	Clock	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	↑	L	H	L
H	H	↑	H	L	H
H	H	L	X	Q	Q

Latches timing and control signals RAS, CAS, LATCH1, LATCH2, ABO AND BHE, clocked by CLK5.

IC	18

74LS10 NAND

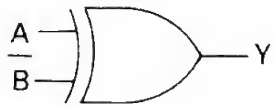


A	B	Y
0	0	1
1	0	1
0	1	1
1	1	0

IC	19

74S86

XOR

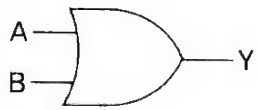


A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

IC	20

74LS32

OR



A	B	Y
0	0	0
1	0	1
0	1	1
1	1	1

4. Mnemonics

Signal	Description	IC	Pin
CLK5	5MHz Clock	18	1
ALE	Address Latch Enable	18	3
CS	Chip Select	20	2
MRDC	Memory Read Control	20	1
WE	Write Enable	16	5
BHE	Bus High Enable	16	14
RAS	Row Address Strobe	17	2
CAS	Column Address Strobe	17	5
LATCH1	Latch1	17	7
LATCH2	Latch2	17	10
DMUX	Data Multiplexer	16	6
AMUX	Address Multiplexer	16	7

5. Parts List

Ref.	Description
IC1 - IC8	HM50256-20
IC9 - IC10	74LS373
IC11 - IC14	74LS257
IC15	74LS163
IC16	74S288
IC17	74LS174
IC18	74LS10
IC19	74LS86
IC20	74LS32
C1 - C6	Cap 0.01 mfd
C7,C14	Cap 100 mfd 6.3V.
D1	Diode OA47
R1	Resistor 3K3 1/4W 3 way SIL Jumper Link
RN1	330/390 Resistor Network Din 4162 64 Pin Plug P.C.B.

4 128K/512K RAM Expansion Board

1. Installation
2. Theory of operation
3. Intergrated circuit catalogue
4. Mnemonics
5. Parts list

1. Installation

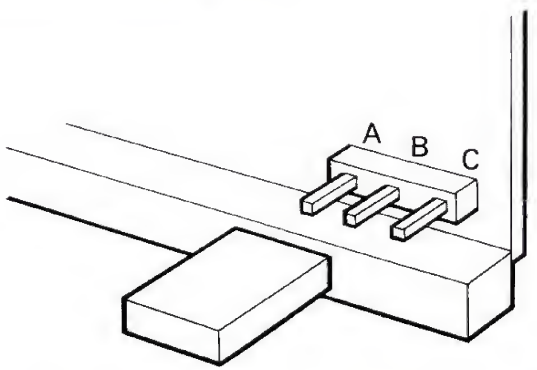
128k Ram or 512K Ram expansion boards may be installed into the Apricot range.

The Apricot PC/Xi range may have 1 or 2 boards fitted making a total capacity of either 384k ,512k or 768k.

> **Note** The F1e ram upgrade is a special 128k ram board with a base address of 128k. The 512K and 256K ram board cannot be fitted at present.

Any expansion slot may be used for individual boards.

A general description of installation procedure is contained at the beginning of this section.



A Jumper P2/P3 is provided to select the base address of the memory board.

P2	256K - 384K	A-B
P3	384K - 512K	B-C
No strap	512K	

2. Theory of operation

The single P.C.B. is designed to use either 64K or 256K drams. This will allow two configurations 128K or 512K.

Data is written directly into the memory with the RAS/CAS addresses being supplied by a single memory controller IC1.

When data is read, it is first latched into IC8 and 9. These latches are gated by IC7 and enabled by MRDC from IC5.

IC3 is a memory controller interface and uses the Apricot control signals to provide RAS/CAS enable. A0 and BHE are decoded to provide CAS enable for the upper and lower memory banks. After data transfer is completed the memory ready signal is returned to the Apricot. A wait state can be introduced by strapping D and E. This will allow slow dram to be used.

The address lines A17-19 are latched into IC4 by ALE and are decoded by IC7 as the base address for IC1's chip select.

Electronic System

Test Points

TP1	on board 5Mhz clock
TP2	ready output
TP3	ALE
TP4	refresh clock.

Straps

A-B	256K - 384K	128K Board
B-C	384K - 512K	
Not fitted	512K	512k Board
D-E	1 wait state for slow drams	

3. Intergrated circuit catalogue

IC No.	Component	Description
1	DP8409	Memory controller
2	DP84300	Memory programmable refresh timer
3	DP84332	Memory controller interface
4	74LS375	4-bit bistable latch
5	74LS244	Octal buffer line driver/receiver
6	74LS74	Dual D-type edge triggered
7A	74LS86	Qual 2-input exclusive -or
8	74LS373	Octal D-type latch
9	74LS373	Octal D-type latch
7B	74S10	Triple 3 input pos nand gate
11-26	4164 - 20	64K/256K drams.

IC	4

74LS375 4 Bit Bistable Latch

Function Table	
Inputs	Outputs
D G	Q Q
L H	L H
H H	H L
X L	Qo Qo

IC4 latches Apricot address lines A17-19 to decode chip select for memory controller address latched by ALE.

IC	5

74LS244 Octal Buffer Line Drive/Receiver

IC5. Tri state buffers used to buffer control signals from expansion bus.

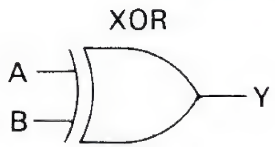
IC	6

74LS74 Dual D-Type Edge Triggered

IC6. Memory ready from IC3 syncronized and clock by Clk5 (5 Mhz). The signal is buffered by IC5 and enabled by Clk5.

IC	7

74LS86 Quadruple 2-Input Exclusive-OR

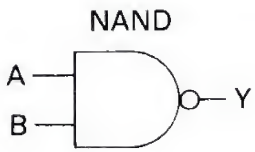


A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

IC7 A/1 fitted on 512K memory boards to decode address lines A18-19 to give chip select for memory controller.

A/2 latches data into octal D-type from drams.

74LS10 3 Input Positive NAND Gate



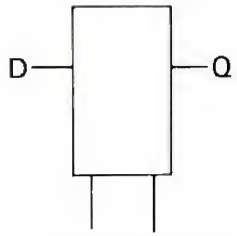
A	B	Y
0	0	1
1	0	1
0	1	1
1	1	0

IC7B/1 fitted on 128K memory boards to decode address lines A17-19 to give chip select for the memory controller.

B/2 latches data from drams into octal buffer.

IC	8,9

74LS373 Octal D-Type Latch



Function Table			
Output Control	Enable G	D	Outputs
L	H	H	H
L	H	H	L
L	L	X	Q
H	X	X	Z

IC 8,9 latches data from drams, gated by NCAS and output enabled by memory read (MRDC).

4. Mnemonics

Signal	Description	IC	Pin No.
A1-19	Address lines		
ALE	Address latch enable	IC5	14
AMWRTC	Advanced memory write command	IC5	16
CLK5	5MHZ clock	IC5	18
A0	Address 0	IC3	2
BHE	Bus high enable	IC3	3
MRDY	Memory ready	IC5	17
MRDC	Memory read command	IC5	9
D0-7	Data bus low	IC9	
D8-15	Data bus high	IC8	
CAS	Column address strobe	IC1	15
RAS	Row address strobe	IC11	4
WE	Write enable	IC11	3

Signal	Description	IC	Pin No.
OE	Output enable	IC9	1
G	Gate enable	IC9	11
R0-8	Row address byte	IC1	
C0-8	Column address byte	IC1	
CS	Chip select	IC1	47
WIN	Write enable input	IC1	45
RGCK	RAS generator clock	IC1	2
RFCK	Refresh clock	IC1	1
RFSH	Refresh	IC1	5
M0	Mode control	IC1	3
RASIN	Row address strobe in	IC1	48
MA0-8	Memory address	IC1	
RFRQ	Refresh request	IC3	8
CASL	Column address strobe lower	IC3	13
CASU	Column address strobe upper	IC3	14
RDY	Ready	IC3	15
WAIT	Wait state	IC3	7

5. Parts list

128K Expansion Board — Part No. 11130511

Comp.Ref.	Item	Part No.	Description	Qty
PC02/02	1	11130411	Printed circuit board	1
IC1	2	11130621	SN74S409 (8409)	1
IC2	3	11130721	IC 20x10 (84300)	1
IC3	4	11130821	IC 16RA8 (84332)	1
IC4	5	11130921	SN74LS375	1
IC5	6	11015121	SN74LS244	1
IC6	7	11131021	SN74LS74	1
IC7	8	11013521	SN74LS10 Fitted in Right Hand Position	1
IC8,9	9	11015521	SN74LS373	2
IC11-26	10	11012521	4164-20 Dram	16
RP1, 2, 3	11	11131221	Res Pak 47R x 4 SIL	3
R1, 5	12	11131321	Res 10ohm 1/4W 10% Carbon	2
R2,3,4,6	13	11017021	Res 3K3 1/4W 10% Carbon	4
C1, 2	14	11131421	Cap 100uF 10V Elec.Axial	2
C3	15	11131521	Cap 1uF 50V 20% Cer.Radial	1
C4-23	16	11131621	Cap 0.1uF 50V 20% Cer.Rad	20
PL abc	17	11131721	3 Way Wafer (22-10-2031)	1
PL de	18	11131821	2 Way Wafer (22-03-2021)	1
Plug	19	11126521	64 Way Conn.DIN 41612	1
TP1-4	20	11131921	4 Way Wafer (22-10-2041)	1
Link	21	11132081	Jumper	1

Modem Board

1. Installation
2. Technical Details

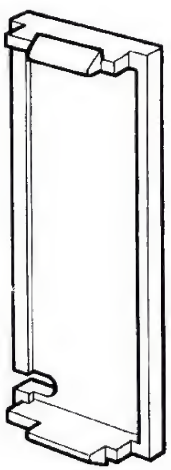
1. Installation

Modem boards may be installed into the Apricot range. If the board is fitted into an Apricot PC or Xi, slot 2 (that nearest to the power supply) must be used.

A general description of installation procedure is contained at the beginning of this section. **Warning - Do Not Connect the Telephone Cord To British Telecom Socket Until The Modem Has Been Correctly Installed In The Apricot Computer**

Warning - This Modem Is Not Suitable For Use With Some Call Connect Systems With Digital Setup And Cleardown Commands.

If the Modem is fitted into the Apricot PC, Xi, F1 or F1e the expansion plate on the rear panel must be removed and the modems telephone cord fed through the resultant hole. The expansion plate must then be replaced by a plate as shown in the diagram below - with a hole to allow the telephone cord to pass through it.



Expansion Plate

If the Modem is fitted into the Apricot Portable the telephone cord may be fed through the cable manager.

When the Modem has been correctly inserted into the machine the approval sticker must be fixed onto the rear panel.

Finally the telephone and Modem must be connected into the telephone socket.

Installation is now complete.

2. Technical Details

Electrical Details:

1. Modulation: Frequency Shifted Keyed (FSK) with the following frequency parameters:

Mode	Baud Rate	Transmit Space	Frequency* Mark	Receive Space	Frequency* Mark	Answer Tone*
CCITT V21						
Originate	300	1180	980	1850	1650	---
Answer	300	1850	1650	1180	980	2225
CCITT V23						
Originate	75/1200	450	390	2100	1300	---
Answer	1200/75	2100	1300	450	390	2100
CCITT V23 Half duplex	1200	2100	1300	2100	1300	2100

* Hz.

2. Data Format: Serial Asynchronous.

3. Minimm Recieve Level: -43dBm.

4. Maximum Transit Level: -13dBm.

Mechanical Details:

1. The Apricot Modem consists of two printed circuit boards linked together.

2. The physical dimensions of the Modem are as follows:

Length;	5.9 inches	(147 mm.)
Max. Height;	3.0 inches	(78 mm.)
Width;	1.1 inches	(27 mm.)
Weight;	7 ounces.	(200 grams)

Connect Details

Series 600 plug for connecting the Modem to the telehone network.

Modem Module

The modem is a communications facility to allow an Apricot computer to transmit and recieve data via the Public Switched Telephone Network (PSTN).

Inspect the modem module to make sure no damage has occured in transit. If damage has occured, return the complete package.

B.A.B.T. Approval No. S/1397/3/E/500039 Model No. ADM/4.

B.T. Circuit

The modem is only to be used with 2 wire PSTN circuits. The modem generates CCITT V25 answer sequences when set in auto answer mode and may be used on lines listed in British Telecom telephone directories. It must not be used with payphones, partylines or certain types of call connect systems that do not use two wire signalling systems.

Bell Tinkle

When the modem is used with telephones that use a mechanical bell 'bell tinkle' will be caused when dialling.

Ringer Equivalence

Equipment for attachment to the public telephone network is assesed to determin its 'ringer equivalence' number (REN). The REN indicates, in effect, the load that the telephone exchange sees when ringing the equipment. It is not permitted to put more than a total of 4 REN onto the exchange line. The modem has a REN of 3 and care must be taken not to use it with other telephone equipment that would result in the maximum figure of 4 REN being exceeded.

Important

The approval of this modem for connection to the British Telecom public switched telephone network is INVALIDATED if the apparatus is subject to any modifications in any way not authorised by BABT or it is used with or connected to:-

1. Internal software that has not been formally accepted by BABT.
2. External control software or external control apparatus which causes the operation of the modem or associated call set-up equipment to contravene the requirements of the standard set out in BABT/SITS/82/005s/B

Local Area Network 6

1. Installation
2. Theory of Operation
3. Connector Pinouts
4. Integrated Circuit Catalogue
5. Mnemonics
6. Parts List
7. Network Diagram.

1. Installation

One local area network board (Lan) can be installed into the Apricot to create a structure so that files/programs can be shared with other people in a local area network.

Any expansion slot may be used for individual boards.

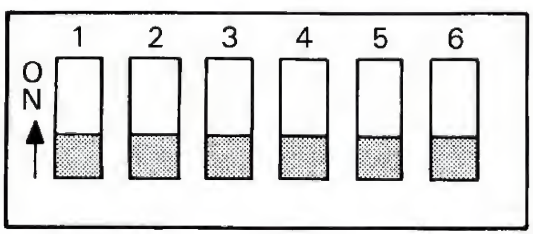
After checking the network device address follow the general installation instructions at the beginning of this section.

When the board has been correctly installed;

1. Connect the lan tap cable to the rear of the lan board.
2. Insert the tap cable into the lan tap box.

Network Device Addresses

The device address is set on a dip switch (SW1) shown as address 63.



Network Device Addresses (SW1)

Address	Switch Setting						Address	Switch Setting					
	1	2	3	4	5	6		1	2	3	4	5	6
0	↑	↑	↑	↑	↑	↑	32	↑	↑	↑	↑	↑	—
1	—	↑	↑	↑	↑	↑	33	—	↑	↑	↑	↑	—
2	↑	—	↑	↑	↑	↑	34	↑	—	↑	↑	↑	—
3	—	—	↑	↑	↑	↑	35	—	—	↑	↑	↑	—
4	↑	↑	—	↑	↑	↑	36	↑	↑	—	↑	↑	—
5	—	↑	—	↑	↑	↑	37	—	↑	—	↑	↑	—
6	↑	—	—	↑	↑	↑	38	↑	—	—	↑	↑	—
7	—	—	—	↑	↑	↑	39	—	—	—	↑	↑	—
8	↑	↑	↑	—	↑	↑	40	↑	↑	↑	—	↑	—
9	—	↑	↑	—	↑	↑	41	—	↑	↑	—	↑	—
10	↑	—	↑	—	↑	↑	42	↑	—	↑	—	↑	—
11	—	—	↑	—	↑	↑	43	—	—	↑	—	↑	—
12	↑	↑	—	—	↑	↑	44	↑	↑	—	—	↑	—
13	—	↑	—	—	↑	↑	45	—	↑	—	—	↑	—
14	↑	—	—	—	↑	↑	46	↑	—	—	—	↑	—
15	—	—	—	—	↑	↑	47	—	—	—	—	↑	—
16	↑	↑	↑	↑	—	↑	48	↑	↑	↑	↑	—	—
17	—	↑	↑	↑	—	↑	49	—	↑	↑	↑	—	—
18	↑	—	↑	↑	—	↑	50	↑	—	↑	↑	—	—
19	—	—	↑	↑	—	↑	51	—	—	↑	↑	—	—
20	↑	↑	—	↑	—	↑	52	↑	↑	—	↑	—	—
21	—	↑	—	↑	—	↑	53	—	↑	—	↑	—	—
22	↑	—	—	↑	—	↑	54	↑	—	—	↑	—	—
23	—	—	—	↑	—	↑	55	—	—	—	↑	—	—
24	↑	↑	↑	—	—	↑	56	↑	↑	↑	—	—	—
25	—	↑	↑	—	—	↑	57	—	↑	↑	—	—	—
26	↑	—	↑	—	—	↑	58	↑	—	↑	—	—	—
27	—	—	↑	—	—	↑	59	—	—	↑	—	—	—
28	↑	↑	—	—	—	↑	60	↑	↑	—	—	—	—
29	—	↑	—	—	—	↑	61	—	↑	—	—	—	—
30	↑	—	—	—	—	↑	62	↑	—	—	—	—	—
31	—	—	—	—	—	↑	63	—	—	—	—	—	—
	1	2	3	4	5	6		1	2	3	4	5	6
Address	Switch Setting						Address	Switch Setting					

Switch on=Logic zero

↑ = on
— = off

The above table displays the switch settings for all devices. The address range is split into three areas:

Address	Device
0-9	File Server
10-63	Network Station
63	Network Bank

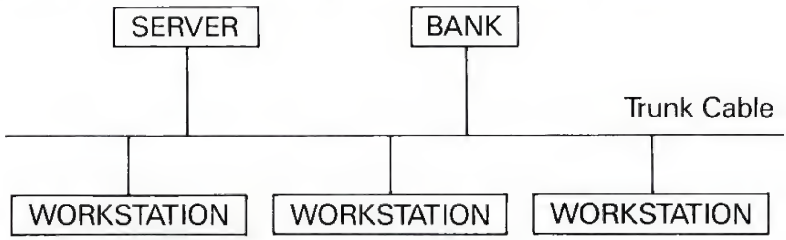
Each network device must have a unique device address.

Maximum bit transfer rate 1M bit/sec.

2. Theory Of Operation

Omninet

The network is based on RS 422, this protocol is used to achieve a high signaling rate over long distances. The trunk cable is a twisted pair and provides a balanced circuit.



Trunk Cable

Data is transferred along the trunk cable from one transporter to another by NRZI (non return to zero inverted).

All data information which travels over the network is in the form of a packet.

Leading Flags	Message Header	User Control	User Data	CRC	Trailing Flags

Network Controller

The design utilizes the corvus chipset which consists of an MC 6801 microprocessor, the MC 68A54 communications controller and a corvus gate array.

6801 Microprocessor
The 6801 is an eight bit microprocessor containing 2048 bytes of rom which stores the transporter operating program and 128 bytes of ram which are utilized for temporary storage by the program.

68A54 advance data link controller (ADLC)
The ADLC provides the interface between the RS422 tranceivers and the transporter. The main functions of the ADLC are bit serialization, zero insertion, packet framing, CRC generation and data byte buffering.

Corvus gate array
The gate array provides the timing and control for all data transfers occuring outside the 6801.

The connection to the trunk cable is via IC7, a RS422 transceiver which provides a balanced circuit for transmitting and receiving data. The driver accepts data bits from the ADLC and converts them into voltage differentials on the lines.

The led is used to indicate when the transporter is transmitting.

An open collector driver IC8 and SW1 (6/8 position dip switch) is used to set the node address and is read once at power on. Each address should be unique.

The 8 bits of data are latched to and from the computer data bus by IC9. The direction and enable is controlled by PAL2.

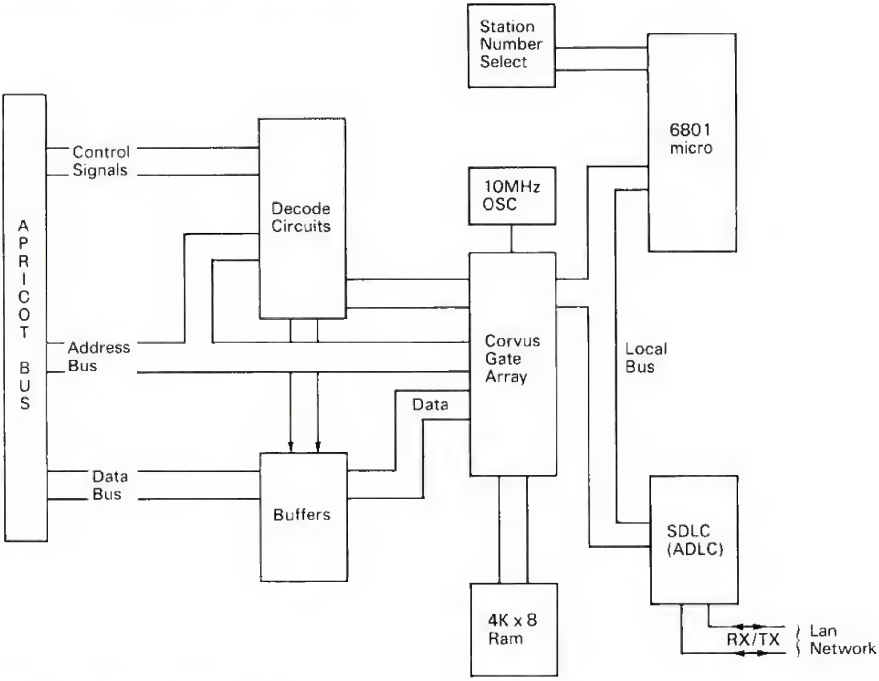
PAL2 decodes the address lines AB5 and AB8 to provide the base address 120H, these addresses are latched by ALE and the read/write status is controlled by IORC/AIOWC.

A 4K byte ram IC4/IC5 is used to store information from the host until required for transmission by the LAN controller. The opposite applies for data from the network to the host.

Network I/O Address

Function	I/O Address	Read/Write Status
Read high nibble of counter and status bit	120H	Read
Read ram location pointed to by counter	122H	Read
Read low byte of counter	124H	Read
Read ram and then increment counter	126H	Read
Write high nibble of counter	120H	Write
Write to command address register	122H	Write
Write to low byte of counter	124H	Write
Write to ram and then increment the counter	120H	Write

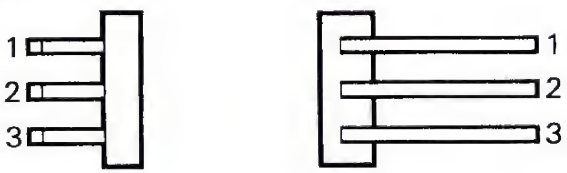
Block Diagram LAN Board



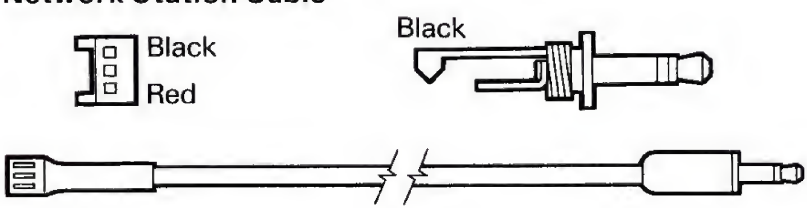
Board Block Diagram

3. Connector Pinouts

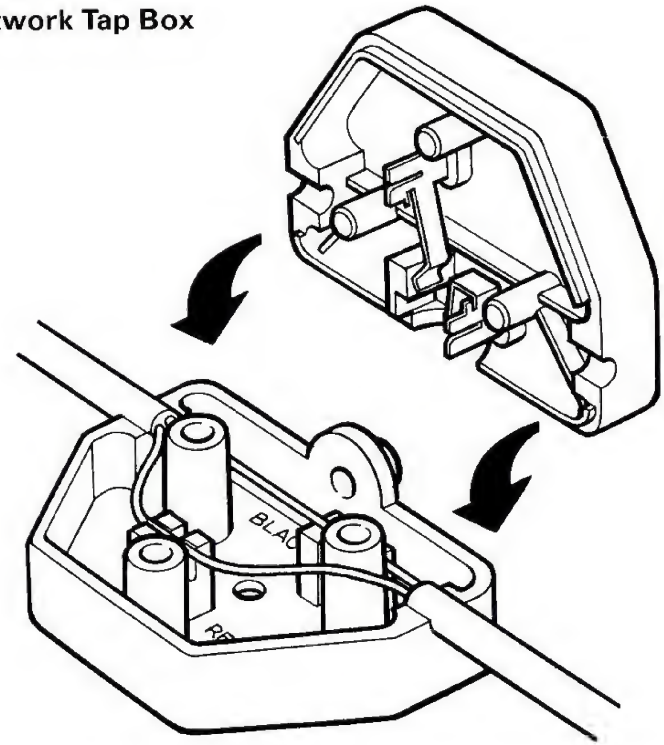
Lan Board



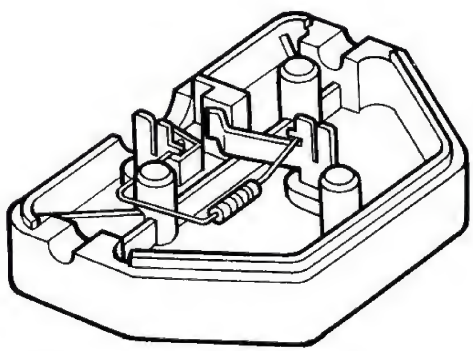
Network Station Cable



Network Tap Box



1. Standard station node box
   Trunk cable should be a continious length where possible.
2. Termination box at each end. The termination box can be used as a standard node.



Network Cable

Cable Lengths

Cable	Network	Between Nodes	Beldon Cable Type Number
Unscreened	2000ft/620m	2m	8205

Tap Cables

Part Number	Length	Function
11114841	3m	Apricot to Apricot

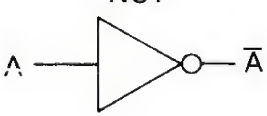
4. Integrated Circuit Catalogue

IC No.	Component	Description
IC1		Corvus gate array
IC2	6801	Corvus processor
IC3	68A54	Corvus ADLC
IC4	6116	Skinny dip ram
IC5	6116	Skinny dip ram
IC6	TBP24510	Prom
IC7	SN75176	RS422 line driver
IC8	SN74LS05	Hex inverter
IC9	SN74LS00	Quad pos-nand
IC10	SN74LS04	Hex inverter
IC11	SN74LS245	Octal bus transceiver.

IC	8, 9

74LS04
74LS05

NOT

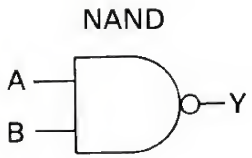


Hex Inverters

In	Out
0	1
1	0

IC	10

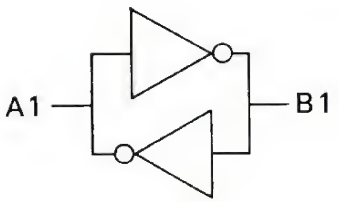
74LS00 Quad Positive NAND



A	B	Y
0	0	1
1	0	1
0	1	1
1	1	0

IC	11

Octal Bus Transceiver



Function Table		
Enable G	Direction Control DIR	Operation
L	L	B Data to A Bus
L	H	A Data to B Bus
H	X	Isolation

IC11 bi-directional data bus from Apricot expansion bus to corvus gate array.

IC	7

SN75176 RS422 Balanced Line Driver

IC7 connects the twin twisted pair LAN network to the LAN board balanced non polorized signal.

IC	4, 5

6116 Skinny Dip Ram

5. Nmemonics

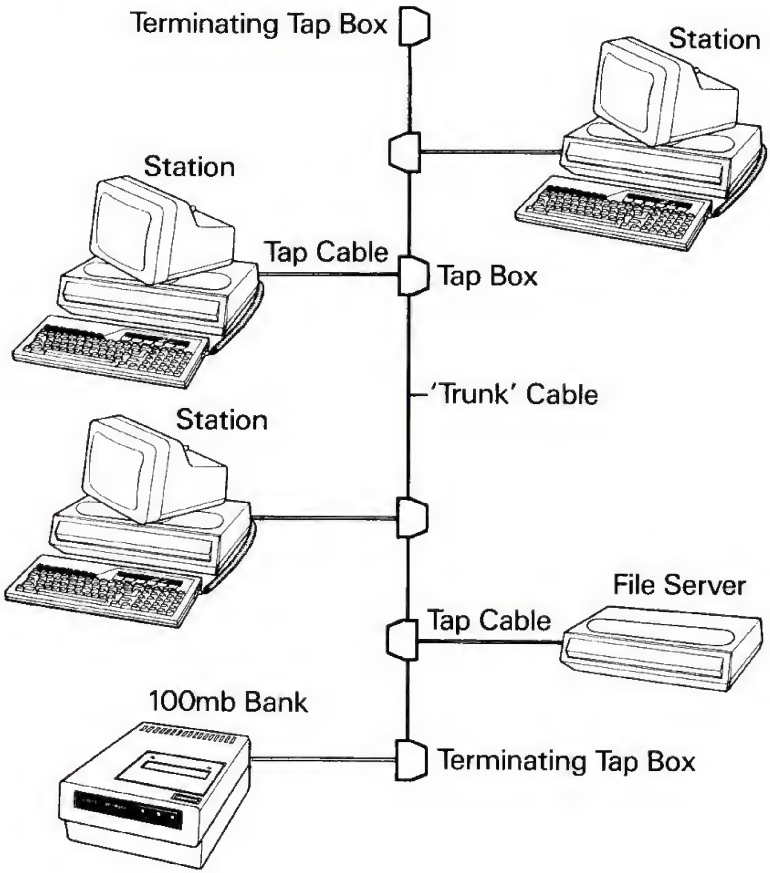
Signal	Description	IC	Pin
AB0-8	Address bus 0-8	IC6	
AIOWC	Advanced I/O write command	IC6	9
IORC	I/O read command	IC6	8
DB0-7	Data bus 0-7	IC9	
INT3	Interupt 3	IC6	20
RESET	Reset	IC2	6
WE	Write enable	IC1	2
CS	Chip select	IC11	20
BRD	Buffer Read	IC6	14
ALE	Address latch enable	IC6	7
RA0-1	Ram Address	IC1	
RD0-7	Ram Address	IC1	
OE	Output enable	IC1	3
WR	Write request	IC1	4
HD0-7	Host Data	IC1	
TXENA	Transmit enable	IC1	61
RXD	Receive data	IC1	62
BITCK	1 MHz clock output	IC1	63
DSR	Data service request	IC1	55
RTS	Request to send	IC1	59
IN/OUT	Transfer IN or OUT of memory	IC1	64
EOUT	1.25 MHz clock output	IC1	57
IRQ	Interrupt request	IC1	60
XTAL2	5 MHz clock	IC1	58
EIN	1.25 MHz clock IN	IC1	56
R/W	Read/Write	IC1	50
AUTO	Decodes which DMA mode is to begin	IC1	65
READY	Ready	IC2	17
A8-15	Address lines	IC2	
HDINT	Interrupt signal to host	IC2	18
XTAL1	Crystal Oscillator 10Meg	IC2	2
RDSR	Receive data service request	IC3	23
TDSR	Transmit data service request	IC3	24
TXC	Transmit data clock	IC3	5
RXC	Receive data clock	IC3	4
DCD	Data carrier detect	IC3	27
CTS	Clear to send	IC3	28
TXD	Transmit data	IC3	6

6 Parts List

Local Area Network Board Assembly Part No. 11156011

Comp.Ref.	Item	Part No.	Description	Qty.
PC08	1	11138611	Printed Circuit Board	1
IC1	2	11156121	Corvus Gate Array	1
IC2	3	11156221	6801 Microprocessor	1
IC3	4	11156321	68A54 ADLC	1
IC4, 5	5	11133221	HM6116ALSP	2
IC6	6	11138921	TBP24S10N AM27521A (alternative) N825129N (alternative) DM745287 (alternative)	1
IC7	7	11139021	SN75176 or DS3695	1
IC8	8	11138721	SN74LS05	1
IC9	9	11013121	SN74LS00	1
IC10	10	11013321	SN74LS04	1
IC11	11	11015221	SN74LS245	1
XTAL	12	11156421	10MHz Oscillator	1
C1	13	11125521	Cap 47uF 10V Electrolytic	1
C2-C11	14	11019021	Cap 0.1uF Decoupler	10
C12	15	11139421	Cap 220pF Ceramic	1
R1-4, R7-8	16	11017321	Res 1K 1/4W Carbon	6
R5, 6	17	11156521	Res 4K 1/4W 10% Carbon	2
T1	18	11156621	Transformer PTABT	1
Q1	19	11140021	Transistor BC184	1
D1	20	11139521	Miniature LED	1
SW1	21	11139221	DIP Switch	1
J1	22	11126521	64 Way DIN 41612 Conn	1
J2	23	11139921	3 Way Conn (22-05-2031)	1
SK1	24	11138821	68 Way Socket	1
SK2	25	11139321	40 Way Socket	1
	26	11139681	Washer M2.5	2
	27	11139781	Nut M2.5	2
	28	11139881	Screw M2.5	2

7. Network Diagrams



Basic (Unbranched) Network Configuration

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